In the Claims:

Please amend claims 1, 3, 10, 14, 15; and cancel claims 2 and 4, without prejudice; and add new claim 30. The status of the claims is as follows.

1. (Currently Amended) A processor adapted to receive instructions in one of ~~having:~~

~~respective~~ first and second external instruction formats ~~in which instructions are received by the processor~~, each instruction specifying one of a plurality of first operations executable by the processor or one of a plurality of second operations executable by the processor, the processor comprising:

at least one execution unit which receives instructions in an internal instruction format and executes the operations specified thereby; and

at least one instruction translation unit which translates each instruction received in at least one of said external formats into such an instruction in said internal format, the internal-format instruction specifying the same operation as the external-format instruction ~~having an opcode which specifies an operation to be executed, and~~;

wherein each said external format has ~~having~~ one or more preselected opcode bits in which an ~~the~~ opcode, specifying the operation to be executed, appears;

at least one said preselected opcode bit of said first external format is a common opcode bit which is also one of said preselected opcode bits of said second external format;

~~an internal instruction format into which instructions in the external formats are translated prior to execution of the operations;~~

~~wherein:~~

~~the operations comprise a~~

each said first operation is specifiable in both said first and second external formats, and each said ~~a~~ second operation is specifiable in said second external format;

all said first operations and all second operations have distinct opcodes in said second external format; and

for every one of the first operations which the processor is capable of executing, the instruction specifying that operation in said first external format is identical, in each said common ~~preselected~~ opcode bit ~~which the first and second external formats have in common~~, to the instruction specifying that ~~the opcodes of the first~~ operation in said second ~~the two~~ external format~~s are identical~~.

2. Canceled

3. (Currently Amended) A processor as claimed in claim 1, also adapted to receive instructions in ~~having:~~ a third external instruction format ~~in which instructions are~~

~~received by the processor, each instruction having an opcode which specifies an operation to be executed, and,~~ said third external format having one or more preselected opcode bits in which an ~~the~~ opcode, specifying the operation to be executed, appears, at least one said preselected opcode bit of said third external format being a further common opcode bit which is also one of said preselected opcode bits of said second external format ;

wherein the or each said execution unit receives instructions in at least one of ~~respective~~ first and second internal instruction formats and executes the operations specified thereby; ~~into which instructions in the external formats are translated prior to execution of the operations;~~

~~wherein:~~

each said second operation is specifiable in both said second and third external formats;

said at least one instruction translation unit translates an instruction specifying said first operation in either said first or second external format ~~is translated~~ into said first internal format, and translates an instruction specifying said second operation in either said second or third external format ~~is translated~~ into said second internal format; and

for every one of the second operations which the processor is capable of executing, the instruction specifying that operation in said second external format is identical, in each said further common ~~preselected~~ opcode bit ~~which the second and third external formats have in common~~, to the instruction specifying that ~~the opcodes of the second~~ operation in said third ~~the two~~ external formats ~~are identical~~.

4. (Canceled)

5. (Original) A processor as claimed in claim 1, being a VLIW processor, wherein one external format is a scalar instruction format used for scalar instructions, and another external format is a VLIW instruction format used for VLIW instructions.

6. (Original) A processor as claimed in claim 1, being a VLIW processor, wherein the external formats are or comprise two different VLIW formats.

7. (Original) A processor as claimed in claim 6, wherein the two different VLIW formats are used in different respective instruction slots of a VLIW instruction parcel.

8. (Original) A processor as claimed in claim 6, wherein at least one instruction slot of a VLIW instruction parcel uses the two different VLIW formats.

9. (Currently Amended) A processor as claimed in claim 1, wherein ~~one~~ said first external format has an instruction width different from that of ~~another~~ said second external format.

10. (Currently Amended) A processor as claimed in claim 1, wherein ~~having~~:

said at least one ~~a~~ translation unit ~~which~~ performs a predetermined translation operation to translate each said external-format opcode into a corresponding internal-format opcode.

11. (Original) A processor as claimed in claim 10, wherein said translation operation involves selecting and/or permuting bits amongst said preselected opcode bits in the external-format instruction.

12. (Original) A processor as claimed in claim 10, wherein the translation operation is independent of the external-format opcode.

13. (Original) A processor as claimed in claim 12, wherein the translation unit identifies the internal format into which each external-format instruction is to be translated, and carries out said translation operation according to the identified internal format.

14. (Currently Amended) A machine-readable medium storing instructions to be executed by a processor,

the processor being adapted to receive instructions in one of ~~Processor instructions encodings having:~~

~~respective~~ first and second external instruction formats ~~in which instructions are received by the processor~~, each instruction specifying one of a plurality of first operations executable by the processor or one of a plurality of second operations executable by the processor,

and the processor comprising:

at least one execution unit which receives instructions in an internal instruction format and executes the operations specified thereby; and

at least one instruction translation unit which translates each instruction received in at least one of said external formats into such an instruction in said internal format, the internal-format instruction specifying the same operation as the external-format instruction ~~having an opcode which specifies an operation to be executed, and~~;

wherein each said external format has ~~having~~ one or more preselected opcode bits in which an ~~the~~ opcode, specifying the operation to be executed, appears;

at least one said preselected opcode bit of said first external format is a common opcode bit which is also one of said preselected opcode bits of said second external format;

~~an internal instruction format into which the processor instructions in the external formats are translated prior to execution of the operations;~~

~~wherein:~~

~~a~~ each said first operation ~~executable by the processor~~ is specifiable in both said first and second external formats, and each said ~~a~~ second operation ~~executable by the processor~~ is specifiable in said second external format;

all said first operations and all second operations have distinct opcodes in said second external format; and

for every one of the first operations which the processor is capable of executing, the instruction specifying that operation in said first external format is identical, in each said common ~~preselected~~ opcode bit ~~which the first and second external formats have in common~~, to the instruction specifying that ~~the opcodes of the first~~ operation in said second ~~the two~~ external ~~formats are identical~~ format.

15. (Currently Amended) A method of encoding processor instructions for a processor, the processor being adapted to receive instructions in one of ~~having respective~~ first and second external instruction formats ~~in which instructions are received by the processor~~, each instruction specifying one of a plurality of first operations executable by the processor or one of a plurality of second operations executable by the processor,

and the processor comprising:

at least one execution unit which receives instructions in an internal instruction format and executes the operations specified thereby; and

at least one instruction translation unit which translates each instruction received in at least one of said external formats into such an instruction in said internal format, the internal-format instruction specifying the same operation as the external-format instruction ~~having an opcode which specifies an operation to be executed, and~~;

wherein each said external format has ~~having~~ one or more preselected opcode bits in which an ~~the~~ opcode, specifying the operation to be executed, appears~~,~~;

at least one said preselected opcode bit of said first external format is a common opcode bit which is also one of said preselected opcode bits of said second external format;

~~the processor also having an internal instruction format into which the processor instructions in the external formats are translated prior to execution of the operations, and the operations comprise a~~

each said first operation is specifiable in both said first and second external formats, and each said ~~a~~ second operation is specifiable in said second external format, said method comprising:

encoding all said first operations and all second operations with distinct opcodes in said second external format; ~~and~~

encoding the opcodes of the first operation in said first and second external formats so that, for every one of the first operations which the processor is capable of executing, the instruction specifying that operation in said first external format is identical, in each said common ~~preselected~~ opcode bit ~~which the first and second external formats have in common~~, to the instruction specifying that ~~the opcodes of the first~~ operation in said second ~~the two~~ external format~~s are identical~~; and

storing the instructions having the encoded opcodes on a machine-readable medium.

16. (Withdrawn) A method of encoding instructions for a processor having two or more external instruction formats and one or more internal instruction formats, the method comprising:

(a) selecting initial encoding parameters including a number of effective opcode bits in each external and internal format and a set of mapping functions, each said mapping function serving to translate an opcode specified by said opcode bits in one of the external formats to an opcode specified by said opcode bits in the, or in one of the, internal formats;

(b) allocating each operation executable by the processor an opcode distinct from that allocated to each other operation in each external and internal format in which the operation is specifiable, the allocated opcodes being such that each relevant mapping function translates such an external-format opcode allocated to the operation into such an

internal-format opcode allocated to the operation and such that all the internal-format opcodes allocated to the operation have the same effective opcode bits; and

(c) if in the allocation (b) no opcode is available for allocation in each specifiable format for every one of said operations, determining which of said encoding parameters is constraining the allocation (b), relaxing the constraining parameter, and then repeating the allocation (b).

17. (Withdrawn) A method as claimed in claim 16, wherein each said mapping function involves selecting all bits of the external-format opcode as some or all of the bits of the internal-format opcode.

18. (Withdrawn) A method as claimed in claim 16, wherein in the selection (a), for each external and internal format, said number of effective opcode bits is made equal to a minimum possible number of opcode bits that could theoretically encode the number of operations specifiable in the format concerned.

19. (Withdrawn) A method as claimed in claim 16, wherein the allocation (b) comprises a series of iterations, and prior to commencing the series of iterations a set of available opcodes in each external and internal format is formed, and in each iteration of the series one said operation is considered and the allocation of the opcode to the considered

operation is made based on an examination of the sets of available opcodes in each external and internal format in which the considered operation is specifiable.

20. (Withdrawn) A method as claimed in claim 19, wherein, for each said external and internal format, the set of available opcodes formed prior to commencing a series of iterations has a number of members dependent upon said number of effective opcode bits currently applicable to that format.

21. (Withdrawn) A method as claimed in claim 19, wherein the available opcodes in all the sets have the same working number of bits.

22. (Withdrawn) A method as claimed in claim 21, wherein said working number is set equal to a minimum possible number of opcode bits that could theoretically encode the number of operations specifiable in the external or internal format having the highest number of operations specifiable in the format concerned.

23. (Withdrawn) A method as claimed in claim 19, wherein each said iteration of the allocation (b) comprises:

(b-1) determining which, if any, available opcodes are common to the sets for all the external and internal formats in which the considered operation is specifiable; and

(b-2) if the determination in (b-1) is that one or more such available opcodes are common, selecting the or one of the common opcodes, allocating it to the considered operation, and removing the selected opcode from the set for each external and internal format in which the considered operation is specifiable.

24. (Withdrawn) A method as claimed in claim 23 wherein each said iteration of the allocation (b) further comprises:

(b-3) if the determination in (b-1) is that no common available opcode is present in the sets for all the external and internal formats in which the considered operation is specifiable, making all existing allocated opcodes void and carrying out the determination and relaxation (c).

25. (Withdrawn) A method as claimed in claim 16, further comprising:

(d) after all of the operations have been allocated one of said available opcodes having said working number of bits, determining for each external format whether that working number is greater than a minimum number of bits needed to provide each operation specifiable in that external format with its own distinct opcode and, if so, restricting the allocated opcodes in that external format to the determined minimum number of bits.

26. (Withdrawn) A method as claimed in claim 25, wherein the operations in (d) comprise:

(d-1) identifying for each external format a maximum-length common prefix, if any, for all allocated opcodes in the external format concerned; and

(d-2) removing the identified common prefix from all the allocated opcodes in the external format concerned; and

(d-3) adjusting each mapping function that serves to translate an opcode specified by the opcode bits in the external format concerned into an opcode specified by internal-format opcode bits so that the mapping function prepends the identified common prefix to the external-format opcode bits during translation.

27. (Withdrawn) A method as claimed in claim 16, wherein if the determination in (c) is that the number of effective opcode bits in one of the external or internal formats is the constraining parameter, the number of effective opcode bits in that format is increased.

28. (Withdrawn) A method as claimed in claim 16, carried out by an electronic data processing device.

29. (Withdrawn) A computer-readable recording medium storing a program which, when executed, encodes instructions for a processor having two or more external instruction formats and one or more internal instruction formats, said program comprising:

(a) a selecting code portion which selects initial encoding parameters including a number of effective opcode bits in each external and internal format and a set of mapping functions, each said mapping function serving to translate an opcode specified by said opcode bits in one of the external formats to an opcode specified by said opcode bits in the, or in one of the, internal formats;

(b) an allocating code portion which allocates each operation executable by the processor an opcode distinct from that allocated to each other operation in each external and internal format in which the operation is specifiable, the allocated opcodes being such that each relevant mapping function translates such an external-format opcode allocated to the operation into such an internal-format opcode allocated to the operation and such that all the internal-format opcodes allocated to the operation have the same effective opcode bits; and

(c) a determining code portion which, if no opcode is available to the allocating code portion for allocation in each specifiable format for every one of said operations, determines which of said encoding parameters is constraining the allocation in step (b), and relaxes the constraining parameter, and then causes the allocating code portion to repeat the allocation of opcodes.

30. (New) A propagated signal embodying instructions to be executed by a processor, the instructions comprising first and second external instruction formats, each instruction specifying one of a plurality of first operations executable by the processor or one

of a plurality of second operations executable by the processor, the processor being adapted to receive instructions in one of first and second external instruction formats, each instruction specifying one of a plurality of first operations executable by the processor or one of a plurality of second operations executable by the processor, wherein the instructions, when executed by a processor, cause the processor to perform the steps of:

receiving the instructions in an internal instruction format and executing the operations specified thereby; and

translating each instruction received in at least one of said external formats into such an instruction in said internal format, the internal-format instruction specifying the same operation as the external-format instruction;

wherein each said external format has one or more preselected opcode bits in which an opcode, specifying the operation to be executed, appears;

at least one said preselected opcode bit of said first external format is a common opcode bit which is also one of said preselected opcode bits of said second external format;

each said first operation is specifiable in both said first and second external formats, and each said second operation is specifiable in said second external format;

all said first operations and all second operations have distinct opcodes in said second external format; and

for every one of the first operations which the processor is capable of executing, the instruction specifying that operation in said first external format is identical, in each said common opcode bit , to the instruction specifying that operation in said second external format.